ABSTRACT OF THE DISCLOSURE

The layout of the semiconductor storage circuit is generated by placing, along a word line direction, a desired number of a circuit extension units each of which includes a data access circuit section, memory cell sub arrays and a power circuit section arranged along a bit line direction. The data access circuit section is driven by a driver circuit provided in the data access circuit section, and the driving operation of the driver circuit is controlled by a driver circuit provided in a control circuit section. Also, a voltage supplying operation of the power circuit section is controlled by a driver circuit provided in a power control circuit section.